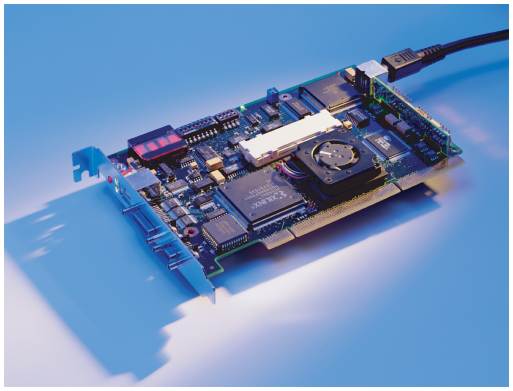
Agilent Technologies E2929B
PCI-X Exerciser and Analyzer

Technical Overview



Key Specifications

- 0 to 133.4 MHz clock speed
- 64 bit data and addressing
- Exerciser (option #300) with full capabilities, including split transactions and 1MB data memory and real-time data generator
- Unidirectional data path verification
- Real time data compare
- Fully PCI-X compliant
- 53 PCI-X protocol rules
- USB, RS-232, external 4MB fast host interface
- Controllable in-system through PCI-X
- Plug-on PCI-X state logic analyzer (option #100) with 2M state trace memory
- PCI-X Performance Optimizer (option #200)
- Realtime and post processed performance analysis
- System Validation Pack (option #310) with compliance tests
- C-API
- FuturePlus FS2104 for connection to Agilent logic analyzers
- Protocol Permutator and Randomizer software (Option #320)

Agilent Technologies

Agilent E2929B PCI-X Exerciser and Analyzer

The E2929B PCI-X Exerciser and Analyzer provides R&D and QA engineers with a fast and predictable way to debug, optimize and validate PCI-X based designs, like servers, motherboards, chip-sets, RAID systems or network interface cards. The modular test card combines a PCI-X protocol checker, a PCI-X exerciser (option #300) with full requester and computer capabilities to generate any kind of PCI-X transfer and a PCI-X state logic analyzer (option #100). In addition, a logic analyzer adapter (FuturePlus FS2104) is available, adding PCI-X protocol check and analysis capabilities to your Agilent 16700 LA.

Individual software modules address specific needs during design bring up, design validation and compliance testing.

Verification of PCI-X protocol compliance

The E2929B features a PCI-X protocol checker, which runs constantly, checking for PCI-X protocol rule violations in real-time. In total, 53 protocol rules are checked concurrently. All rules are derived from the PCI-X and PCI specification. Thus, just plugging the E2929B into a PCI-X system and activating the protocol rule checker allows you to check for PCI-X protocol compliance. The E2929B reports a list of all the errors that have occurred. For the purpose of debugging, the protocol checker can be used to trigger either the plug on state logic analyzer (option #100) or an external logic analyzer. Also, each individual protocol rule can be masked.

Predictable system and chip validation

The E2929B PCI-X Exerciser (option #300) features a fully controllable requester and computer, real-time data compare and the Agilent patented Protocol Permutation and Randomizing technique. This allows engineers to validate and stress the PCI-X system with specific and fully repeatable test cases.

Efficient design debugging

To get an insight into your system, a simple click of the mouse is all that is needed to setup a specific trigger or the PCI-X plug-on state analyzer (option #100). Alternatively, you can connect the E2929B to your Agilent 16700 Logic Analyzer system using the FuturePlus FS2104 logic analyzer link.

The plug-on PCI-X state analyzer offers impressive trigger and storage qualifier capabilities. This makes it easier to find complex error conditions. Besides conventional pattern terms for all PCI-X signals, an additional bus observer makes the current bus status (e.g. address phase, attribute phase, data phase, idle phase etc.) transparent, and thus simplifies the setup of trigger conditions. Combining additional error pattern terms, external trigger inputs and trigger sequencer capabilities, the E2929B gives you the ultimate power to capture the data you need.

System benefits

Easy PCI-X system evaluation

- Windows based GUI for interactive use
- Plug-on PCI-X optimized state analyzer
- Optimize design and test corner cases
- PCI-X Exerciser stresses your system's corner cases predictably and repeatedly
- Easy system validation using ready to run tests
- Over 1,000,000 test cases in less than 5 seconds[1]
- Programmable In-System
- C-Application Programming Interface

System overview

The E2929A is a short PCI-X card, which can simply be plugged into the system under test. It is controlled by an interactive Graphical User Interface or from a specific customer C Program (option #320 required). The software can either be installed on the system under test itself - controlling the E2929B through the PCI-X system bus, or on an external host - controlling the E2929B either by USB, RS-232 or a 4MB/s fast host interface, designed for a high data transfer speed.

1 test case @133MHz = (50 clocks delay + avg. 250 clocks for 2k bursts) *7.5ns = 2.5us. Thus, 1,000,000 test cases need = 2.5s + 2s setup time.

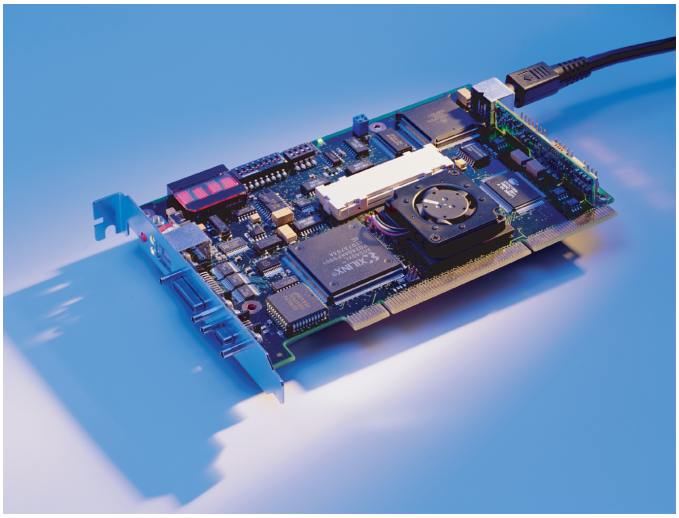


Figure 1: E2929B

PCI-X Protocol Checker

The E2929B basic configuration supports the PCI-X protocol checker which checks 53 PCI-X protocol rules in real-time. Each rule can be individually masked to suppress the triggering of known problems. The rules are derived from the PCI-X specification[2] , and are designed to find any possible violations of the PCI-X protocol. When a protocol violation is detected, the protocol checker can:

- store the rule number of the first (non-masked) violated rule
- list all found protocol errors
- accumulate the number of violated rules
- directly trigger the plug-on PCI-X state analyzers trace memory (option #100)
- directly trigger the FuturePlus FS2104

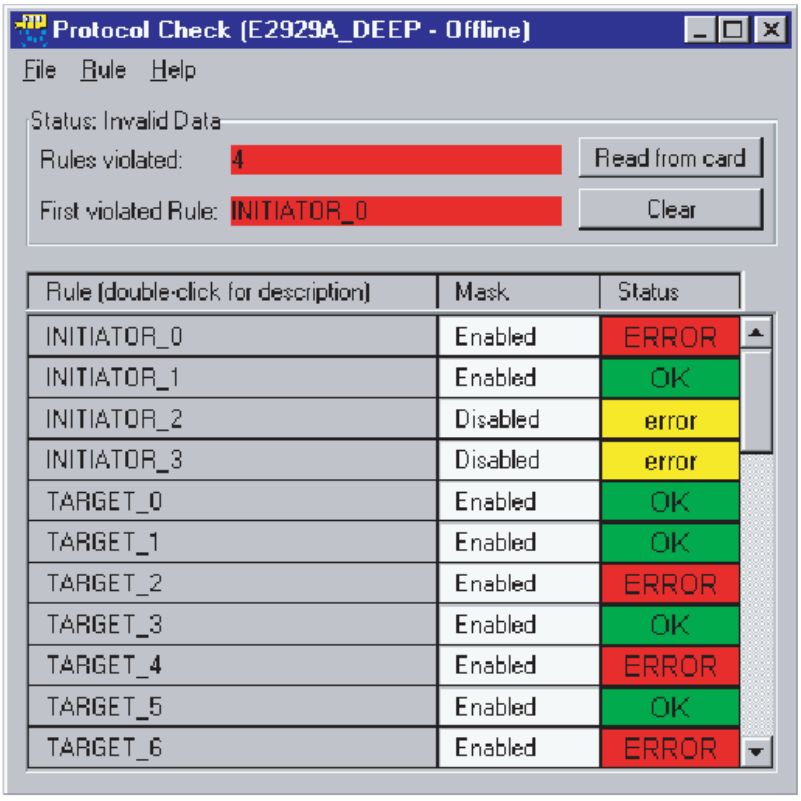


Figure 2: Protocol Checker

2 PCI-X Addendum to the PCI Local Bus Specification Revision 1.0, September/22/1999

List of Protocol Rules and Description	Reference
An initiator can terminate a transaction with master abort (deassert FRAME# and IRDY#) 8 clocks after the address phase(s).	PCI-X Spec 2.11.1.2.
If the target inserts wait states on burst write or Split Completion, the initiator must toggle between its first and second data values until the target asserts TRDY# (or terminates the transaction).	PCI-X Spec 1.10.2. Rule 5
The initiator is required to terminate the transaction when the byte count is satisfied.	PCI-X Spec 1.10.2. Rule 6
The initiator is permitted to disconnect a burst transaction (before the byte count is satisfied) only on an ADB.	PCI-X Spec 1.10.2. Rule 7
Burst Write and Split Completion transactions must not be terminated with Split Response. All other target terminations are permitted.	PCI-X Spec 2.6.1.
The target is permitted to signal Single Data Phase Disconnect only on the first data phase (with or without preceding Wait States).	PCI-X Spec 1.10.3. Rule 6
The target is permitted to signal Split Response only on the first data phase (with or without preceding Wait States).	PCI-X Spec 2.11.2.4.
Once the target has signaled Disconnect on Next ADB, it must continue to do so (or signal Target Abort) until the end of the transaction.	PCI-X Spec 2.11.2.2.
The target deasserts DEVSEL#, STOP# and TRDY# one clock after the last data phase (if they are not already deasserted) and floats them one clock after that.	PCI-X Spec 1.10.3. Rule 8
There must be an even number of target initial wait states for a burst write and Split Completion.	PCI-X Spec 2.9.
If a PCI-X target signals Data Transfer (with or without preceding Wait States), the target is limited to disconnecting the transaction only on an ADB (until the byte count is satisfied).	PCI-X Spec 1.10.3. Rule 5
FRAME# cannot be deasserted unless IRDY# was asserted	PCI Spec Appendix C, Rule 8c
When FRAME# has been deasserted, it cannot be reasserted during the same transaction.	PCI spec Appendix C Rules 8b and 8d
IRDY# must be asserted two clocks after the attribute phase.	PCI-X Spec 1.10.2. Rule 3b
Initiator Wait States are not permitted	PCI-X Spec 1.10.2. Rule 3b
A transaction starts when FRAME# is asserted for the first time. IRDY# must not go low when FRAME# is high.	PCI Spec Appendix C, Rule 7 and 8c
Once asserted IRDY# must stay asserted until the end of transaction or till the target signals a termination.	PCI-X Spec 1.10.2. Rule 3b and PCI-X Spec 2.9.
TRDY# must not be asserted before the attribute phase, but two or more clocks later.	PCI-X Spec 2.8. Table 2-6 and PCI Spec Appendix C Rule 14
Once TRDY# has been asserted, it must not be deasserted and reasserted during the same transaction (no subsequent wait states).	PCI-X Spec 1.10.3. Rule 4
DEVSEL# must be asserted prior to the edge at which the target asserts TRDY#.	PCI-X Spec 2.8. and PCI-X Spec 2.9.1.
DEVSEL# must not be asserted during a special cycle or if a reserved command has been used.	PCI-X Spec 2.4. and PCI-X Spec 2.7.3.
DEVSEL# must not be asserted 1, 5 or more than 6 clocks after the address phase.	PCI-X Spec 2.8.
After a Target asserts DEVSEL#, it cannot be deasserted until the last data phase has completed, except to signal Data Transfer, Wait States, Target Abort, Split Response, Retry and Single Data Phase Disconnect.	PCI-X Spec 1.10.3 Rule 3
DEVSEL# must be deasserted one clock after last transfer.	PCI-X Spec 1.10.3 Rule 8
STOP# must not be asserted without DEVSEL# being asserted, except RST# being asserted.	PCI-X Spec 1.10.1.Rule 12; PCI spec Appendix C, Rule 14, spec 6
If the target signals Split Response, Target-Abort or Retry, the target must do so within eight clocks of the assertion of FRAME#.	PCI-X Spec 1.10.3 Rule 4
If the target signals Single Data Phase Disconnect, Data Transfer or Disconnect on Next ADB, the target must do so within 16 clocks of the assertion of FRAME#.	PCI-X Spec 1.10.3 Rule 4
ACK64# may only be asserted, when REQ64# was asserted before (ACK64# is a response to REQ64#).	PCI Spec 3.8.
A 64-bit initiator asserts REQ64# with the same timing as FRAME# to request a 64-bit data transfer. It deasserts REQ64# with FRAME# at the end of the transaction.	PCI-X Spec 2.12.3. Requirement 4
If a 64-bit target is addressed by a transaction that does have REQ64# asserted with FRAME#, the target asserts ACK64# with DEVSEL# to complete the transaction as a 64-bit target. It deasserts ACK64# with DEVSEL# at the end of the transaction.	PCI-X Spec 2.12.3.
REQ64# must not be used with special cycle or interrupt acknowledge command. Only burst transactions (memory commands other than Memory read DWORD) use 64-bit data transfers.	PCI-X Spec 2.4. and 2.7.
For DWORD Transactions, REQ64# must be deasserted.	PCI-X Spec 2.12.3. Requirement 2
PERR# may never be asserted three clocks after the address phase (or earlier in a transaction) or during a special cycle. During WRITE, PERR# may be asserted three clocks after IRDY#, during READ, PERR# may be asserted three clocks after TRDY#.	PCI Spec 3.8.2
AD[31::0] address parity error	PCI Spec Appendix C, Rule 32 b
AD[63::32] address parity error	PCI Spec Appendix C, Rule 32 c
AD[31::0] data parity error occurred but was not signaled.	PCI-X Spec 5.3.
AD[63::32] data parity error occurred but was not signaled.	PCI-X Spec 5.3.
AD[31::0] data parity error occurred	PCI Spec Appendix C, Rule 32 b
AD[63::32] data parity error occurred.	PCI Spec Appendix C, Rule 32 c
For I/O and DWORD Memory transactions, AD[1::0] and byte enable encoding must have a defined relationship. See table 2-2 in the PCI-X Spec.	PCI-X Spec 2.3, table 2-2
Reserved commands are reserved for future use.	PCI-X Spec 2.4
DAC is not allowed immediately after a DAC.	PCI Spec 3.9. and PCI-X Spec 2.12.1.
During the data phases C/BE# bus must be driven high for all Burst Transactions except Memory Write.	PCI-X Spec 2.6.
During a Dual Address Cycle, a 64-bit master has to drive the upper half of the address on AD[63::32] in the initial and in the second address phase.	PCI-X Spec 2.12.1.3 a i)
In the second address phase of a Dual Address Cycle, AD [63:32] and AD [31:0] contain duplicate copies of the upper half of the address.	PCI-X Spec 2.12.1.3 a i)
During a Dual Address Cycle, a 64-bit master has to drive the bus command on C/BE [7::4]# in the initial and the second address phase.	PCI-X Spec 2.12.1.3 a ii)
In the second address phase of a Dual Address Cycle, C/BE [7::4]# and C/BE [3::0]# contain duplicate copies of the transaction command.	PCI-X Spec 2.12.1.3 a ii)
DWORD Transactions only support a single data phase.	PCI-X Spec 2.7.
A master that supports 64-bit addressing must generate a SAC instead of a DAC, when the upper 32 bits of the address are zero. This rule detects a bus hang. If the bus does not get idle once within 4095 clocks, it triggers. *Implementation note*: The counter can be programmed between 1...4095 clocks. A value of 0 for the counter turns the rule off.	PCI spec 3.9 Agilent Rule to detect potential deadlocks.
A master did not respond to a split transaction within 2^{20}-1 clocks. *Implementation note*: The counter can be programmed between 1...2^{20}-1 clocks. A value of 0 for the counter turns the rule off.	Agilent Rule to detect potential deadlocks.
A delayed transaction (retries) has not yet been repeated within 2^{15} clocks.	PCI spec 3.3.3.3.3
A delayed transaction has not terminated within 2^{16} clocks.	Agilent Rule to detect potential deadlocks

Plug-on PCI-X state analyzer (Option #100)

The plug-on PCI-X state analyzer observes all signals (except JTAG) specified by the PCI-X specification for a 64 bit 66/100/133MHz system. The analyzer runs at a clock speed of 0 to 133,4 MHz.
In detail, the analyzer captures:

- 2M samples
- all 64 bit PCI-X address/data signals
- PCI-X protocol errors
- bus observer to decoded bus state signals, time aligned to the bus signals
- active requester-initiator and requester-target signals, aligned with the bus signals for easy identification of transactions involving the exerciser
- 4 signals from the trigger I/O connector

Storage qualification

A simple push-button storage qualification selects storage qualified to tune the use of the state analyzer memory, depending on the level of detail you need. For example:

- store all states
- suppress idle cycles
- suppress wait cycles
- suppress data transfers
- by pattern term

The storage qualification can also be user programmed, using the trigger sequencer.

7 Pattern terms

The E2929B provides a total of 8 pattern terms:

- 2 pattern terms monitoring all PCI-X bus signals (excluding JTAG signals) and trigger inputs
- 1 pattern term monitoring the protocol checker error signals, spilt transaction errors and data compare errors
- 4 pattern terms monitoring the bus observer

To set up a pattern, each individual bit can be masked 0/1/X. For bit fields, such as C/BE, all bit combinations can be defined individually.

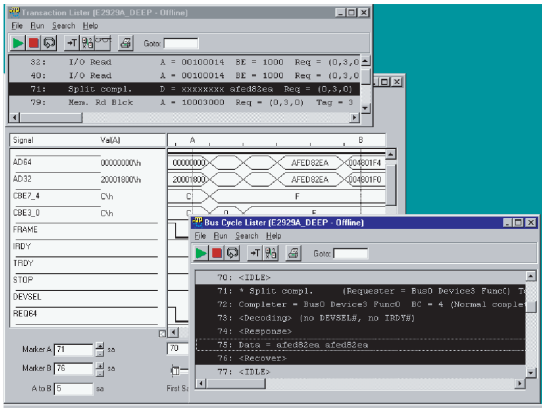


Figure 3: Waveform viewer: Bus cycle lister and transaction lister with cross references.

Bus observer for easy triggering

The bus observer allows easy triggering for the engineer's daily tasks by defining only one simple pattern term. This is because the bus observer automatically detects:

- idle bus cycles
- address cycles, the 1st and 2nd half of dual address cycles respectively
- attribute phase
- transactions to 32 or 64 bit address space
- decode cycles, decode speed A/B/C/subtractive
- data cycles
- 32 or 64 bit transfers
- target responses as claim transactions, single data phase disconnection, disconnection of next address boundary, abort
- split transactions / response
- waits and retries
- master aborts
- terminated unsuccessful transactions

16 level trigger sequencer

For extended trigger scenarios, the E2929B features a trigger machine, which flexibly handles up to eight pattern terms, one termination counter (pre-load and decrement) and up to 16 levels of trigger sequencing.

Sequence levels	Available Patterns/ counter
1	up to 7
2	up to 6
3..4	up to 5
5..8	up to 4
9..16	up to 3

Pattern terms can be combined with logical operations AND, OR and NEGATION. The termination counter can be pre-loaded and decrement.

Flexible trigger points

For maximum flexibility, the trigger can be placed in any position in the trace memory.

External trigger I/O

4 trigger I/O signals provide a way to synchronize between multiple PCI / PCI-X test cards of the E2920 Series, REQ# and GNT# lines of other PCI / PCI-X devices or other test equipment like a general-purpose logic analyzer. Programmed as input pins, they are observed by the state analyzer and are available as part of the pattern terms.

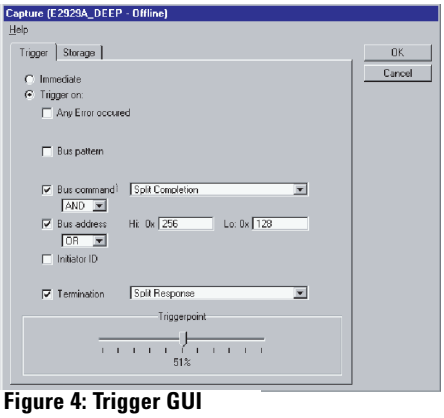


Figure 4: Trigger GUI

GUI or C-API control

The plug-on PCI-X state analyzer comes with a Windows based GUI (Graphical User Interface) and CLI (Command Line Interface). It can be controlled through the optional C-API (option #320).
The Command Line Interface (CLI) allows you to interactively control the PCI Exerciser and Analyzer by entering command functions that correspond with the functions provided by the C-API. The CLI can also process batch files of concatenated command functions.

FuturePlus PCI-X Analysis Probe[3]

With the FuturePlus PCI-X Analysis Probe, the E2929B PCI-X protocol checker becomes an integrated part of your 16700 logic analyzer system. With the Analysis Probe, which is simply plugged onto the E2929B, each PCI-X signal is passed to the 16700 logic analyzer system, together with a protocol error signal. This is the optimum solution whenever cross-correlation between the PCI-X bus and other system interfaces is needed for efficient system debugging or software development. The Analysis Probe and E2929B are controlled by the logic analyzer. The probe features:

- connectors to the 16700 logic analyzer
- dip switches to mask individual PCI-X protocol errors
- LED bank to indicate individual protocol errors
- protocol checker reset
- FuturePlus analysis software running on the Agilent 16700 logic analyzer systems.

Whenever the probe is connected to the E2929B, the E2929B automatically switches into continued PCI-X protocol error check and bus sampling mode. Thus, set-up is as easy as plugging the E2929B into the PCI-X slot and connecting the logic analyzer.

PCI-X Performance Optimizer (option #200)

This optional package extends the Agilent E2929B with performance measurement capabilities. Using the PCI-X Performance Optimizer in-depth post processed statistical performance analysis can be done. For this analysis, one or multiple bus snapshots are taken by the PCI-X analyzer.

Optimize system performance

Statistical PCI-X Performance analysis makes it easy to select the best PCI-X cards and components, detect and locate PCI-X performance bottlenecks, and balance system settings so that the overall performance of the system is optimized.

A hierarchical approach to analyzing post-processing performance measurements is used. This means that the Agilent E2929B can move swiftly from high-level throughput numbers to, for example, PCI-X command usage and latency measurements, as required. It is therefore simple to identify design issues and analyze their causes. Overall, this approach reduces the effort required in revealing design problems.

- Graphical and text-based presentation
- In-depth performance analysis through post-processing
- First word latency measurement
- Reveals completer and requester contribution to performance measurement results
- Split statistics
- Measures overall traffic and selective for requester/completer pair
- Report generation
- Cross-references to PCI-X Analyzer Graphical User Interface

Post-Processed Data Analysis

The E2929B can carry out an in-depth performance analysis of sampled PCI-X transactions by using the PCI-X Analyzer to acquire data.

Basic bus statistics

To obtain an overall picture of the PCI-X performance, the PCI-X bus is analyzed for:

- PCI-X throughput
- PCI-X utilization
- Average first word latency
- PCI-X efficiency
- Average split rate
- PCI-X data efficiency

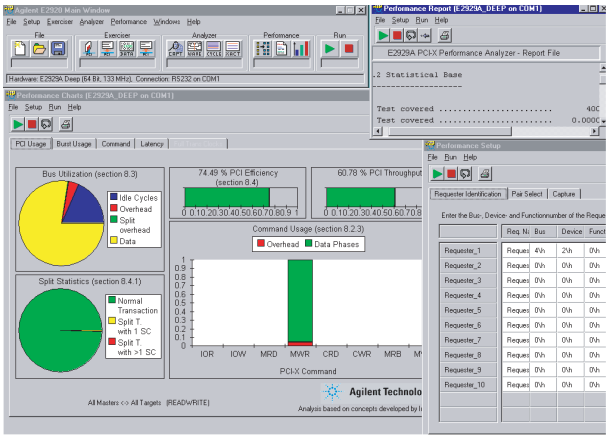


Figure 5: Performance Windows: setup, report and charts

[3] The analysis probe is not an Agilent product. Agilent works closely with FuturePlus to ensure quality products. But the vendor is responsible for functionality, pre-sales and post-sales support and warranty

A bus efficiency chart provides an overview of how efficiently the traffic was handled between different bus agents.

Bus utilization
The bus utilization analysis shows how the PCI-X bus was used by:

- data transfer
- overhead

A utilization chart shows how the different bus agents used the bus.

Requester/Completer Performance
Post-processing allows the analysis of customer-selected requester/completer combinations so that specific requester/completer performance behavior can be analyzed in depth. By evaluating the critical agents using the real-time measurements and basic bus statistics, the in-depth requester/completer analysis provides an "inside view" of how to optimize single agents.

Latency Histogram
A latency histogram shows the fraction of transfers that had a certain sequence length and first word latency.

Split Transaction Statistics
Number of split sequences and average values of first word latency, length and time overhead as well as a statistic of pending requests over time.

Overhead Statistics
States if requester or completer was the cause of a certain fraction of overhead.

Burst length distribution
This histogram also shows the distribution of burst length over PCI-X commands. Again, this provides an "inside view" into performance bottlenecks in PCI-X systems. This is observed per sequence as well as per transaction.

Command usage chart
The command usage chart lists the usage of different PCI-X commands so that performance issues caused by inefficient command usage are revealed.

Requester/completer efficiency
A further important indication for PCI-X system performance is how efficiently a certain requester/completer pair uses the occupied bus time. Thus, the software examines:

- requester/completer overall efficiency of transferred data
- efficiency over burst length.

Termination statistics
The PCI-X termination statistics indicate:

- termination over command.
- cause of termination (imitator/target) over burst length.

Report and Result ASCII-File
All results are available as an ASCII report file for further analysis and customer post-processing.

The different segments are:

1 GENERAL INFORMATION
  1.1 Test Base
  1.2 Statistical Base

2 BASIC BUS STATISTICS

3 BUS THROUGHPUT STATISTICS

4 EFFICIENCY STATISTICS
  4.1 Requester Completer Efficiency
  4.2 64 Bit Bus Statistics

5 BUS UTILIZATION STATISTICS
  5.1 Requester Completer Utilization

6 BUS USERS OVERVIEW7 SPLIT TRANSACTION
  STATISTICS
  7.1 Pending requests over time

8 REQUESTER - COMPLETER PAIR:

<Requester selected by user> <-> <Completer selected by user>
  8.1 Statistical Base
  8.2. Bus Utilization
    8.2.1 Data Phase
    8.2.2 Overhead
    8.2.3 Command usage, observed per sequence
    8.2.4 Command termination, observed per transaction
    8.2.5 Bytecount over command, observed per sequence.
    8.2.6 Bytecount over command, observed per transaction
  8.3 Efficiency Statistics
    8.3.1 Efficiency over bytecount
  8.4 Termination Statistics
    8.4.1 Split statistics
    8.4.2 Termination Burst histogram, observed per transaction
  8.5 Latency Histogram

  8.5.1 Top 10 list of first word latencies

Real Time Performance GUI

In the bring-up and debug phase of a PCI-X device or a system (containing PCI-X bus and PCI-X devices), it is necessary to evaluate the performance of the device or system under test.

The Agilent PCI-X E2920 software supports real-time performance measurement by providing predefined, standardized performance measurements, such as PCI-X efficiency and PCI-X utilization.

The Real Time Performance GUI is included as part of the software package for the E2929B card.

PCI-X Exerciser (option #300)

The Agilent E2929B has an optional on-board 64 bit PCI-X exerciser. The exerciser operates at 0 to 133.4 MHz, and can emulate and force practically any behavior of a PCI-X device imaginable- except blatant protocol violations. The exerciser comes with a graphical user interface (GUI) and a command line interface (CLI). As an option, the exerciser can be controlled from a C-API (option #320). The exerciser features:

- two requester queues
- one computer
- four completer queues to handle independent split-transactions
- one requester-target handling up to 32 open requests

Requester and computer are fully programmable, operate independently of each other and are able to handle:

- 32/64 bit data transfers
- 32/64 bit addressing
- programmable delays between transactions
- block length up to 4Gbyte
- all 16 PCI-X command types

Configuration space

The E2929B provides configuration space, which is fully programmable. Default values (customizable) are stored in an EEPROM on-board and are used to initialize the configuration space when the power is on. The configuration space can be disabled, making the card invisible to BIOS or O/S configuration routines. Thus, analysis tests are possible without having any effect on the device or system under test.

Architectural overview

The exerciser is based on two main ideas. Firstly, defining requester initiator data blocks, describing 'what' data should be transferred and secondly, defining a requester initiator behavior, describing how the transfer should be executed.

For the requester initiator, up to 256 blocks of data transfers can be set up (see figure 2). In addition, requester initiator behaviors are set up, specifying how the requester initiator intends to transfer the data blocks over the PCI-X bus. If any completer target replies to a transfer and requests a split transaction, the requester initiator data block attributes are moved internally to a split transaction map for further use. The transaction map can manage up to 32 open split transactions. When completing split transactions, the requester target behaviors are used to control the transfer.
The completer target behavior attributes define how the completer target of the E2929B acts. The completer target can manage up to 4 split transaction queues. It is also possible to fully control initiating the completion of split transactions. The completer initiator behavior attributes are used to program it. The programmable transaction scheduler decides whether completer or requester transaction is performed. All data comes or goes through the on-board data memory or from the on-board real-time data generator.

Requester Initiator data block

The requester initiator data block settings define which address space is accessed, and where data is moved. Up to 256 block transfers can be defined and performed in a linear sequence by one of the two transfer queues. Each block specifies:

- the bus command seen on C/BE[3::0] in the address phase. All valid PCI-X commands are supported
- the 64 bit bus address
- the byte enable value (C/BE[3::0] / C/BE[4::7]
- the start address of the data memory or if the data generator is used
- the number of bytes to be transferred (1 to 4GB)
- if the real-time data compare for incoming data should be activated
- the start condition for the transfer (immediately or wait for event)
- the transfer queue the data is passed through

Requester Initiator behavior

The requester initiator behaviors are set to specify the PCI-X transfer behavior per address/data phase. Up to 256 attribute entries, which can be setup as linear sequence or repeat loops, are allowed.
The attributes control:

- 32 or 64 bit data access
- insertion of 1 to 65535 clock cycles delay between transactions
- the next data queue to be used
- if an automatic or customer defined tag (0..31) is used

- the specific burst length for the transfer (1 to 4096 byte) automatically rounded up to the next qword boundary
- the n-th ADB where the requester initiator disconnects (1 to 32)
- perform 0 to 4 address steps
- how many clock cycles after the address phase REQ# is de-asserted (0 to 2047)
- how often the current transfer attributes are used (repeat value 1 to 256)

Latencies between requester initiator transactions

The latencies between transactions can be varied using requester initiator behavior property. The minimum latency is in general ≤1 clock cycle - including any sequences of read/write where real-time data compare is involved. The only exception is if the most recent transaction is a read/write transfer into data memory and the subsequent transaction is a write out of data memory. In this particular case, the latency is 10 to 20 clock cycles.
Please note that it is assumed that the master does not need to disconnect before the byte count of the current sequence is transferred and that wait cycles are added if required by the PCI-X specification.

Requester target behavior

The requester behavior attributes are set to specify the PCI-X transfer behavior per address/data phase if a target requests the completion of a split transaction from a requester initiator. Up to 256 attribute entries, which can be setup as linear sequence or repeat loops, are allowed. The attributes control:

- the decode speed used (A[4] /B/C)
- acknowledgement of 64 bit data transfers
- the number of initial latency clock cycles (3 to 34)
- the behavior after initial latencies, either accept transfer, disconnect, signal retry or abort
- how often the current behavior is applied (repeat value 1 to 65536)

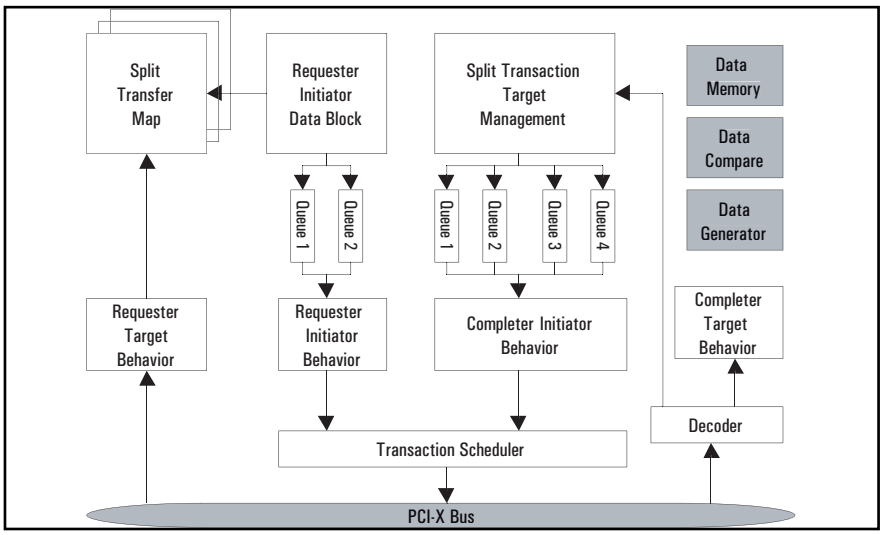


Figure 6: E2929B option #300 PCI-X exerciser architecture

Completer Target behavior attributes

The completer target behavior attributes give full control over the E2929B completer target behavior, and define how it reacts to a request. Up to 256 attribute entries, which can be setup as linear sequences or repeat loops, are allowed. The attributes control:

- the decode speed used (A[4] /B/C)
- acknowledgement of 64 bit data transfers
- the number of initial latency clock cycles (0 to 31)
- the behavior after initial latencies, either accept transfer, signal a single data phase, retry or abort
- the behavior in subsequent data phases, either accept all subsequent data phases, disconnect after 1 to 2047 data phases
- signaling a split response, either by identifying an address value or range in the address phase, the decoder accessed, or by a subset of all 16 possible PCI-X commands
- the split transaction queue to be used
- how often the current behavior is applied (repeat value 1 to 65536)

Configuration space and decoders

In total, the E2929B features 5 decoders:

- one standard configuration space decoder, fully customer programmable
- 3 programmable target decoders (six bars) that can either hold up to 3 memory spaces (64 bit) or 2 memory spaces and 2 I/O spaces simultaneously
- one decoder to access the 64Kbyte expansion ROM

All decoders can be switched off by a dip-switch on the E2929A, making the card completely invisible to the system under test.

Completer Initiator behavior

The completer initiator behavior attributes are set to specify the PCI-X transfer behavior per address/data phase if a completer target starts to complete a split transaction. Up to 256 behavior entries, which can be setup as linear sequence or repeat loops, are allowed.

The attributes control:

- the split transaction queue to be served
- the start condition for this transfer
- 32 or 64 bit data transfer
- the number of clock cycles inserted before REQ# is asserted (1 to 65535)
- the number of clock cycles before REQ# is de-asserted (1 to 2047)
- the number of address steps (2 to 6)
- how often the current transfer attributes are used (repeat value 1 to 256)
- disconnect at n-th ADB (1 to 32)

[4]Decode speed A is supported up to 66 MHz

Completer target latencies
The initial latencies can be programmed with the completer target behavior attributes. Depending on the selected decode speed and address phases, the test card automatically adds the needed number of wait states to achieve the defined initial latency. A minimum of one wait cycle is always added when using decode speed B or C and a minimum of two wait cycles are needed with decode speed A.

In case the subsequent target access is a 'read from target' and the most recent event was a 'write to target', 'read from other target address', 'master write' or 'master read', the minimum initial latency is 15 clock cycles.

Data memory
The E2929B option #300 features a 1MB (128K x 2 dwords) programmable read/write data memory. Master / requester and target/ completer share the memory. The address decoders can selectively address it. The data memory can:
- store data from read/write transfers
- be mapped to any PCI-X address space

Data generator
Instead of using the data memory, the on-board data generator can be used. Without initial latencies, the generator can generate a data pattern, deterministically linked to the data address. Combined with a second exerciser card and the real-time data compare feature, long-time load stressing on any PCI-X to PCI-X data path can be performed while errors are detected in real-time (figure 3).
The generator features the following patterns:
- walking ones or zeros
- ground bounce
- count up (unique data)
- pseudo random pattern (unique data)

The count up and pseudo random pattern are unique up to the length of 1M quad words (4Mb). The data uniqueness is derived out of the lower bit 2 to 22 of the bus address.

Real-time data compare
Real-time data compare can be performed either on:
- Memory:
  when data is written to the memory it is compared against the actual memory content
- Data Generator:
  based on the data address the generator calculates the expected data and compares it with incoming data.

Exerciser Graphical User Interface
The Graphical User Interface gives you an easy way to setup and control the exerciser.

Master conditional start [5]
The master conditional start window allows you to set up the start conditions for the master traffic. Following a run command, the master can be programmed to start:
- immediately
- triggered by a pattern

Target decode window
The target decode window lets you configure the target address decoders. As well as configuring the programmable decoders for the exerciser's on-board memory, you can individually enable or disable the decoders for configuration space and expansion ROM. You can also store the current settings as defaults, which will then be used following all subsequent power cycles or PCI-X resets.

Error Injection Capabilities
The E2929B is capable of injecting error conditions into a system including generating inverted parity (PAR and PAR64), signalling a parity error (PERR#) or a system error (SERR#) in a specified phase of the transaction.

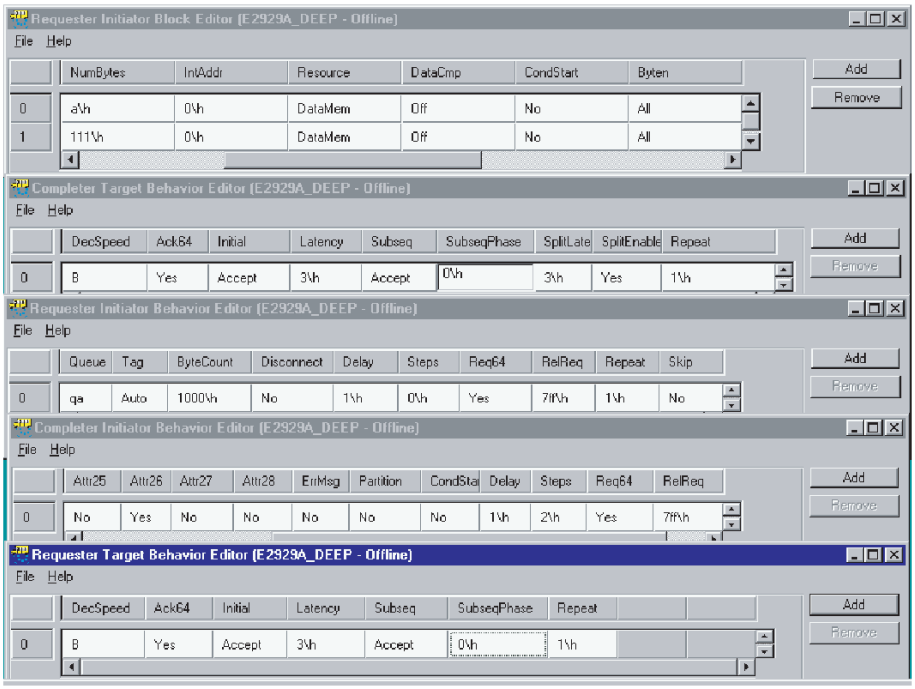


Figure 7: Exerciser GUI

[5] supported by GUI with software revision 2.0

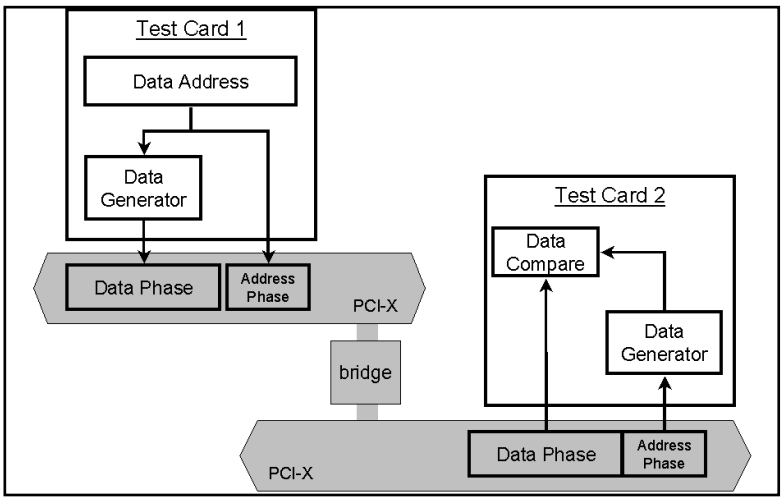


Figure 8: Undirectional data path verification

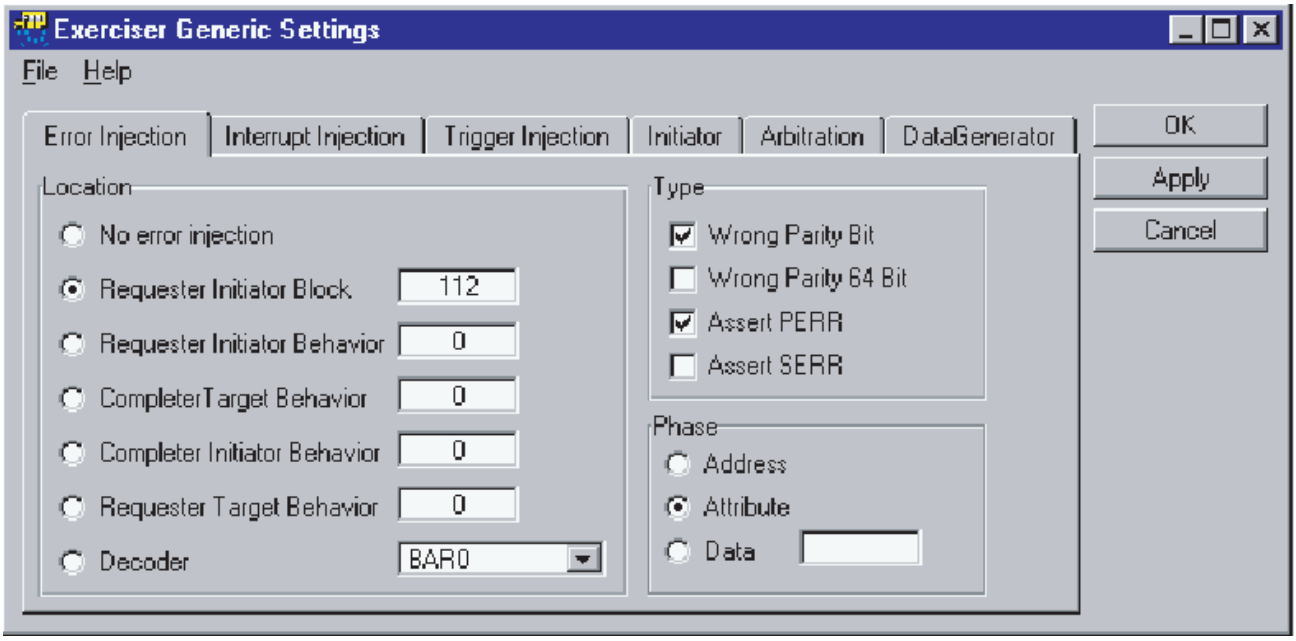


Figure 9: Exerciser Generic Settings

Configuration window

The configuration window lets you view and modify the current configuration space settings of the PCI-X exerciser and analyzer card. You can also store the current settings as defaults, which will then be used following all subsequent power cycles or PCI-X resets.

Data memory editor

The data memory editor lets you view and modify the contents of the exerciser's on-board memory. This allows you to define the data content for master write transfers or target read accesses to the card, as well as allowing you to view the data received from master read transfers or target write accesses. The data can be viewed in hex format, big or little endian, and 8, 16, 32 and 64 bit size.

Data generator setup window

The data generator setup window allows you to select the algorithm to be used for data generation.

Agilent System Validation Package (Option #310)

The System Validation Package is a ready-to-use software package, which performs system stress tests during the validation of servers, workstations, PCs, or other PCI/PCI-X based systems.

With its easy-to-use Windows-based GUI, it simplifies test development on setup for engineers and allows easy test execution by technicians.

Choosing the Agilent E2925B, E2928A, E2940A, E2929B option #310 adds the System Validation Package to your hardware order.

Target application

The System Validation programs and controls multiple PCI/PCI-X Exerciser and Analyzer test cards of the E2920 PCI Series to create realistic application system traffic. The test card approach allows you to set up fully predictable traffic scenarios and gives you measurable test coverage and test predictability. Used for validation of PCI/PCI-X based systems and silicon, it enhances the traditional test method of using off-the-shelf PCI/PCI-X cards.

Outstanding test coverage

Today's validation test methods typically lack time efficiency and repeatable execution of critical system traffic scenarios. Hot mock-up tests, which use off-the-shelf PCI cards to load a system-under-test and wait until an error occurs, are the typical test approaches used today. Now the System Validation executes such types of system critical tests within minutes, simply with a mouse click.

PPR, the key technology

Agilent's Protocol Permutation and Randomizing (PPR) technology is the key to predictable and repeatable test coverage. PPR is technology that allows permutation of the PCI/PCI-X protocol and traffic in a determinisitic way. Thus, system critical test patterns are not only transferred between different system components, but also automatically permutated to achieve all possible traffic scenarios.

Stress all critical data paths

Just by plugging the PCI/PCI-X Exerciser and Analyzer test cards in each individual PCI/PCI-X bus of your system under test, the software is able to automatically test and stress data paths within your system (see Figure 1).

A small executable running on the system CPU(s) allows testing within the whole system, not only the I/O system, while tests are run from an external controlling host.

System Validation Package/System Test Library benefits

- Fully controlled test environment for validation of servers, workstations and PCs
- Predictable test coverage
- Repeatable test scenarios
- Documented test results

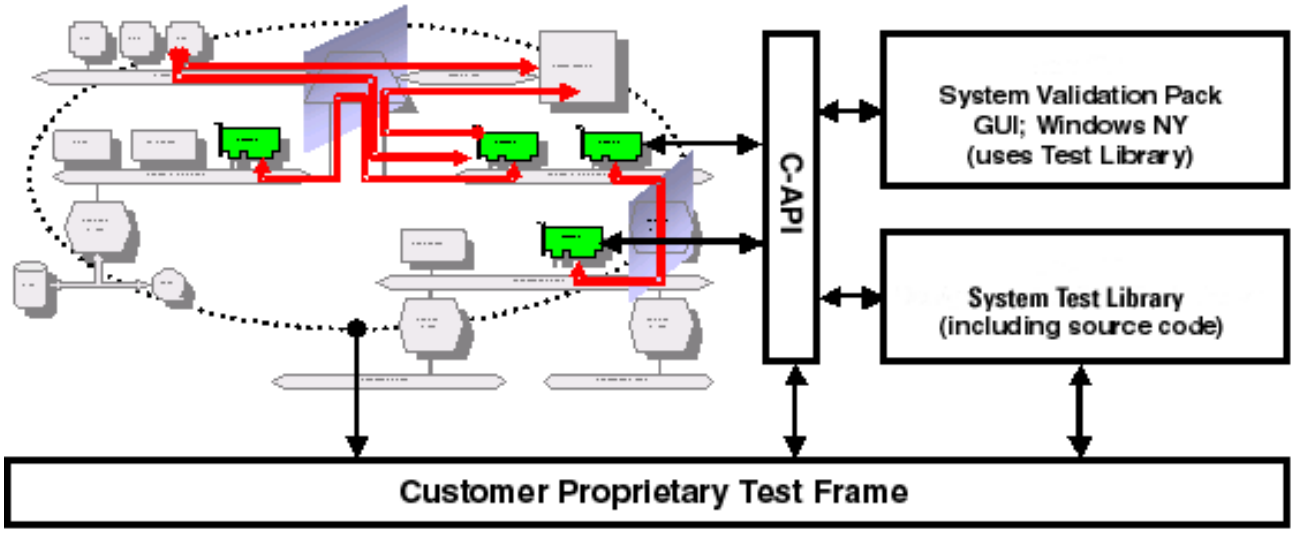


Figure 10. System Architecture

Test method

The Agilent System Validation allows automatic tests and stress data paths from:

- CPU and Exerciser to system memory
- Exerciser to system memory
- CPU to Exerciser memory space
- CPU to Exerciser I/O space
- Peer to peer traffic
- Master to target traffic
- Load generation

While testing, the setup emulates typical traffic scenarios in a PCI system. For example, data CPU to SCSI card, LAN to LAN card traffic, concurrent system memory access from LAN card and CPU (see Figure 2).

So far, these have been typical traffic scenarios and have been generated within the so-called hot mock-up test. Now the Agilent verification solution significantly extends this validation process by:

- Increasing test coverage through increased number of variations, when dealing with system traffic.
- Being programmable to force the system's most critical traffic conditions.
- Being repeatable for failure analysis and failure regression tasks.
- Being comparable, to achieve measurable quality improvements.
- Producing log files to catch the problems before the system hangs.
- Creating test reports to document system quality.
- Making an easy link to R&D's debug environment.

Any access from an Agilent Exerciser is permutated using PPR, varying block sizes, memory commands, alignments, and byte-enables (meaning all variations of dword, word, and byte read/write accesses are used). Protocol variations on all system actions include waits/latency, terminations, 64 bit and 32 bit access, address/data stepping and as well as acceptance/non-acceptance of 64 bit access .

Automatic test setup

When starting the validation software on a system under test, it automatically scans the system for Agilent PCI/ PCI-X Exerciser and Analyzer cards. Based on the available test cards, the operator can select various tests, define the test duration and start the test.

Customer configurable tests

All tests are configurable by the customer. The GUI shows all parameters, and all setups are simply done with a mouse click.

Thus, using different Exercisers to test between different buses, e.g. 33 MHz PCI and 133 MHz PCI-X, is easy. With each test, you just select the path to test. The software automatically communicates with the test card plugged into the corresponding bus and tells you which protocol/traffic parameters you may vary.

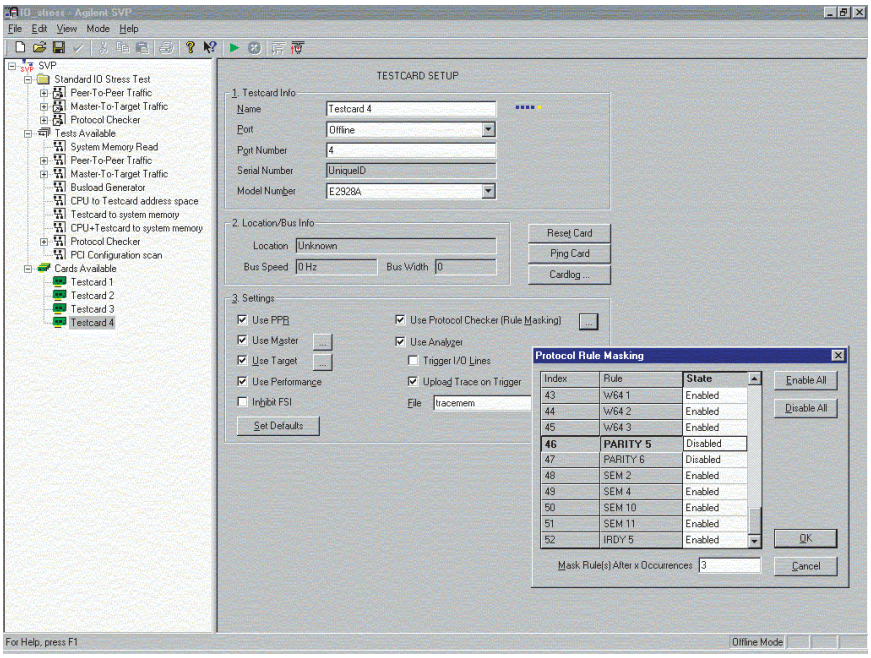


Figure 11. Test card setup

Tests Available

PCISIG Compliance Tests

The Agilent System Validation Package includes a series of tests defined by the PCI Special Interest Group (PCI-SIG).
Agilent Technologies has been working closely together with the PCI-SIG to provide compliance tests, which are utilized, for testing PCI and PCI-X systems at each PCI-SIG Compliance workshop. Agilent supplies the hardware and software to perform PCI-SIG compliance testing, including a PCI-SIG Compliance Test Library. The tests are used to verify that devices and systems are compliant to the PCI and PCI-X specifications. The tests are set up and run via the System Validation Package combined with either the PCI or PCI-X exerciser/analyzer test cards.
These tests are in addition to the standard tests included or part of the System Validation Package option.

Description of the compliance tests:

- MLT - Master Latency Test
This test is not implemented as a special test within SVP but can be carried out manually. To do this, carry out the PCI configuration scan test
(see "PCI Configuration Scan" on page 50) and examine the latency settings to determine the result of this test.

· SIG Post Test

This test is utilized to initialize the Base Address registers and to verify the address assignments. To do this, the test card is defined as target.

· SIG Interrupt Routing Test

The exerciser asserts an interrupt on request from the analyzer mailbox. To do this, the test card is defined as a master.
The SVP software requests an interrupt from the card and verifies that the interrupt was received and processed correctly.

· CPU to Test card Address and Test card to System Memory Address

This test accesses either the memory space or the I/O space of the test card from the CPU. To do this, the test card is defined as a target.
This test also accesses the system memory from the PCI or PCI-X bus. To do this, the test card is defined as a master and sends different write and read commands from/to the analyzer.

· SIG Card Test

The SIG Card test performs a number of tests. This includes testing for:
· Correct values and operation for the Command Register.
· The Status register.
· Appropriate values for other configuration registers.
The configuration register contents are displayed during the SIG Card test in the SVP Reporting window that opens when you run the test.

· PMTEST - Power Management Test

· TYPE1 - Type 1 Test

The Type 1 test verifies correct configuration transaction decoding by the device.

· DISCARD - Discard Test

This test verifies that the card correctly repeats retried PCI transactions.

· DISCARD - Discard Test

This test verifies that the card correctly repeats retried PCI transactions.

For more information about the PCI-SIG Compliance Program and the Agilent System Validation Package, please refer to www.agilent.com/find/pci_SVP or to www.pcisig.com

Further Tests

The following list describes all tests available for the System Validation. All tests are customer configurable (see Table 2, page 12), and stress one data path. All tests can be performed concurrently to increase and maximize stress conditions. The PPR capabilities vary from Exerciser model to Exerciser model. For example, different protocol variations are available for PCI and PCI-X. Please refer to the corresponding technical data sheet of the Exerciser used for a list of available protocol variations.

CPU and Exerciser to system memory

Access system memory space via virtual memory from CPU and from PCI/PCI-X bus (Exerciser acting as master). The same address range with interleaved addresses is used in order to stress cache controller.

- **Tested data paths:** CPU to host memory; Exerciser to host bridge to system memory.
- **Tested devices:** Host bridge and host bridge configuration, host memory controller, and arbitration unit.

W/R/C to System Memory

Access the system memory from the PCI/PCI-X bus, and perform data write/data read/data compare.

- **Tested data paths:** Exerciser to host bridge to system memory
- **Tested devices:** Host bridge, host bridge configuration, host memory controller, and arbitration unit

Read from memory

This test reads repetitively from a customer-defined physical address to check accessibility and to stress the data path:

- **Tested data paths:** Exerciser to host bridge to system memory
- **Tested devices:** Host bridge, host bridge configuration, host memory controller, and arbitration unit

Peer-To-Peer Traffic

Two PCI Exerciser cards access each other's memory or I/O space. Master-target traffic in both directions is set up. Two test cards on different buses are used to test the bridges and bridge configuration.

- **Tested data path:** Exerciser #1 to bridge(s) to Exerciser #2
- **Tested devices:** Bridges, bridge configuration, and arbitration units

Master Target Traffic

Two PCI Exerciser cards access each other's memory or I/O space with unidirectional master-target traffic. Two test cards on different buses are used to test the bridges and bridge configuration.

- **Tested data path:** Exerciser #1 to bridge(s) to Exerciser #2
- **Tested devices:** Bridges, bridge configuration, arbitration units

CPU to test card

This test accesses either the test cards memory or I/O space via virtual memory from the CPU.

- **Tested data paths:** CPU to host bridge to test card
- **Tested devices:** Host bridge, host bridge configuration, host memory controller, and arbitration unit

Bus Load Generation

An Exerciser is set up to generate self-traffic and therefore saturate a bus with a defined level of traffic. This kind of test stresses other devices on the same bus by limiting the available time a certain device can get access to the bus. Also the arbitration unit can be verified under controlled bus load conditions.

Error Analysis

The Analyzer of an E2920 Series test card can be set up to check for:

- Protocol violations
- Data transfer errors
- Parity errors
- Bus hang-ups/bus locks
- Bus load measurements

Detected problems are logged in a report file. Optionally, a trace memory waveform file is generated for in-depth root cause analysis. All PCI/PCI-X devices on the bus are passively observed.

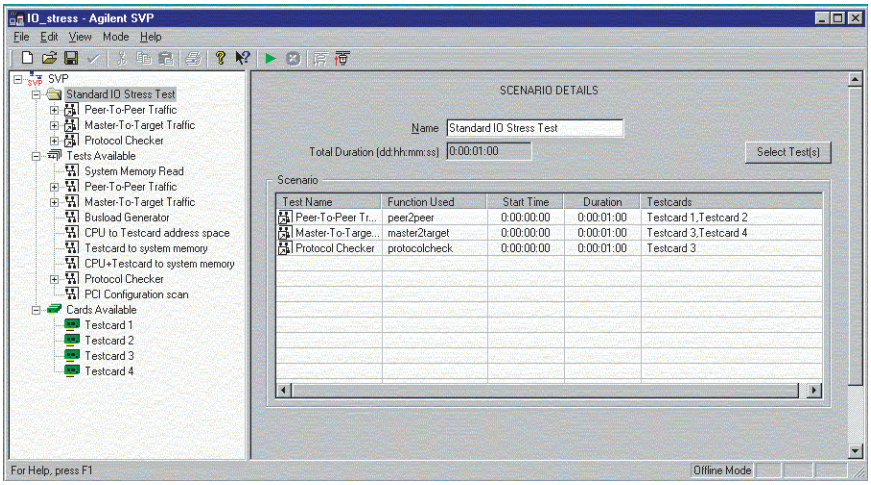


Figure 12. Test scenario setup window

In-system Programmable

The Agilent System Validation can be installed and executed on the system-under-test itself. In this case, the Exerciser and Analyzer are programmed through the PCI and the PCI-X interface.

External Control

Alternatively, the whole test can also be controlled from an external host PC, which runs the System Validation. The Exerciser and Analyzer are connected via an appropriate external interface (RS-232, 4MB fast host interface). To execute a test that requires the FSI (see Table 2), the FSI must be installed on the system under test.

Working with non-Windows OS

Two options are available to verify a system that does not use Windows.

Use an external controlling host PC

In this case, any test which does not require the FSI can be executed immediately. To use the other test, the FSI, which is only a small C-program, must be compiled for the appropriate OS. The FSI is delivered as executable for Windows DOS, and in source code.

Porting the System Test Library

The other alternative is to import the complete System Test Library to your preferred OS. Therefore, the System Test Library comes with source code.

Optionally, special porting support is offered, helping you to incorporate the System Test Library test capabilities into your proprietary test environment.

Table 2. Customer Configurable Test Parameter

			Customer configurable test parameters						Usable mechanisms to detect errors			
	# of cards	FSI[2]	Band-width	PPR	Address Space	Address Prefetch	Address	Memory Size	Data Compare	Protocol Check	Protocol Error Mask	Capture Waveform on Error[3]
CPU and Test Card to System memory	1	yes	1..100%	√	Memory	n/a	by OS	0..512KB/ 0..1MB[1]	√	√	√	√
Peer to Peer Test	2	no	1..100%	√	Memory or I/O	true or false	by BIOS/ OS	0..512KB/ 0..1MB[1]	√	√	√	√
Master/Target Traffic	2	no	1..100%	√	Memory or I/O	true or false	by BIOS/ OS	0..512KB/ 0..1MB[1]	√	√	√	√
CPU to Test Card	≥1	yes	1..100%	√	Memory or I/O	true or false	by BIOS/ OS	0..512KB/ 0..1MB[1]	√	√	√	√
Write/Read/ Compare to System Memory	≥1	yes	1..100%	√	Memory	n/a	by OS	Dword value 0..4Kbyte	√	√	√	√
Read From System Memory	≥1	yes	1..100%	√	Memory	n/a	Address Value	Dword value 0..4Gbyte	√	√	√	√
Bus Load Generation (self traffic)	≥1	no	1..100%	√	Memory or I/O	n/a	by BIOS/ OS	0..512KB/ 0..1MB[1]	—	√	√	√

1. The memory can be specified for the selected Exerciser. 512KB data memory is available on E2925B, E2928A, and E2940A. 1MB data memory is available on E2929B
2. The FSI (Front Side Interface) is a small executable table which must run on the system under test CPU(s).
3. Requires option 100 for the E2929B. Not available for E2922A.

Required E2920 Series Exerciser/Analyzer
The System Validation Package requires a full Exerciser/ Analyzer (see Table 3).

Ordering Information

The System Validation Package can be ordered as option #310 of the E2925B, E2940A, E2928A, and E2929B
The system test is also available as a system test library to be integrated in customer proprietary test frames. Refer to System Test Library technical specifications (5968-3500E) for more information.

Table 3. Minimal Exerciser/Analyzer Configuration Needed for Option #310/System Test Library

	Option #310	System Test Library
E2929B PCI-X Protocol Checker	•	•
#100 (Analyzer)	•	•
#300 (Exerciser)	•	•
#320 (C-API)		•
E2925B/E2940A/E2928A PCI	•	•
#300 (Exerciser)	•	•
#320 (C-API)		•
E2922B PCI-X Master Target Test Cards		• [1, 2]

1. For error detection, the E2922B supports PCI-X protocol and data compare only. Other analyzing capabilities like waveform capture, trigger I/O, or bus load measures require the E2929B.
2. The E2922B does not support external interfaces and must be in-system programmed through PCI-X.

C-API / PPR (Option #320)

The optional C-Application Programming Interface (C-API) provides a programming interface for setting up and controlling the exerciser and analyzer. Option #320 comes with a library of C functions to facilitate control of the exerciser and analyzer. Option #320 also comes with a PCI Protocol Permutation and Randomizing library.

The test program can run on the system-under-test itself or on an external controller. If the program runs on an external host, the Agilent E2929B connects via USB, RS232 or fast parallel port to the external host. If the test program runs on the system-under-test, the PCI-X interface itself is used.

The library functions are divided into groups, which allow you to set up and control the various capabilities of the Agilent E2929B.

Recommended development environment: MS Visual C++ V. 6.0 or higher.

Protocol Permutation and Randomization (PPR)

The PPR library extends the C-API by offering dedicated functions to setup PCI-X protocol permutation in a pseudo random sequence. It allows easy to set up transfers of contiguous blocks of data with as many protocol variations as possible. Therefore, the PPR software calculates which variations are covered, and after how many data transfers, by permutating the possible protocol variations. It determines whether the coverage, within programmed constraints, can be achieved under given test circumstances, and calculates the test time required to perform the data transfers.

Generating permutations

The user-defined protocol constraints can be easily set by specifying lists of protocol variations, which must occur. For example, which different burst lengths, wait cycles, memory read/write commands, etc.
Then, PPR automatically moves simultaneously through the lists. With each step, that is, with each permutation, the next value in this list is combined with the next values in the other lists. The hardware based permutation proceeds in this way until each value of each list is combined with all values of the other list, and thus all combinations are covered. In this way, the repetition or omission of combinations is avoided.

Documented test coverage

A printable report tells you which protocol variation the device has exposed. It explicitly reports which protocol attributes are permutated against which other protocol attributes, and after how many data transfers.

Optimized test time

The values to be varied can be specified for each master and target attribute separately. Thus, focusing on interesting cases can optimize testing time.

By carrying out these protocol permutations in real-time within the exerciser hardware, these tests run much more quickly than any other CPU-based test program.

Effective test generation

The exhaustive C-library makes it simple to focus on test structuring, partitioning and the specification of protocol constraints. This means that an appropriate and valuable test for protocol verification with meaningful results can quickly be obtained. Once started, the test can easily be extended to incorporate newly gained experiences or to address testing needs for newly invented PCI-X features.

Deterministic test conditions

In contrast to PCI-X traffic generated by other PCI-X cards, the generated variations are completely deterministic and reproducible.

Supported protocol variations

The exerciser and analyzer allow the variation constraints for the PCI-X transfer, PCI-X master/requester and PCI-X target/completer behavior to be specified. All specified constraints can be permutated against each other and up to 100 constraints can be maintained per list.

PCI-X transfer variations

The generator features the following algorithms:

- start address alignment; a list of arbitrary address alignments to start PCI-X transfers at given offsets (e.g. 1 dword) relative to the q word boundaries
- byte enables; a list of selected values for the C/BE lines during the address phase
- block size; a block describes a contiguous range in memory available to be transferred. A list of up to 100 different block sizes (from 1 to 4096 byte) can be selected to be transferred
- bus commands; a list of selected PCI-X bus commands. All selected commands are permutated with other selected constraints, as appropriate, for the specified transfer direction and PCI-X specifications
- permutation of release ordering bit
- permutation of no snoop bit.

Target behavior variations

The requester initiator allows for the variation of:

- byte count (1 to 4096)
- disconnect/initiator termination
- delay
- address stepping
- REQ64
- release REQ

The completer initiator allows for the variation of:

- Error message, yes/no
- partitioning
- delay
- address stepping
- REQ64
- release REQ

General Specifications

PCI-X specifications:
PCI-X bus: 32/64 bit
Addressing: 32/64 bit

PCI Clock range:
Analyzer: 0 to 133.4 MHz
Exerciser: 0 to 133.4 MHz

Timing specifications:

	Min.	Max.
T_{val}		3.8 ns
T_{on}	0 ns	
T_{off}		7 ns
T_{su}	1.2 ns	
$T_{su(ppt)}$	1.2 ns	
T_{h}	0.5 ns	

@ temperatures of -40°C to +55°C

The E2929B fully meets timing specifications for 133 MHz PCI-X.

Electrical Specifications:
For 3.3V environment, complies with PCI-X Spec. 1.0.

Decoupling: unused 3.3 V power pins are decoupled.

Power requirements: consumes less than 25 W from PCI-X slot.

Trace length limits:
meets PCI-X specifications.

Signal loading:
less than 10 pF, fully PCI-X compliant.

Operating temperature:
-40°C to +55°C.

Mechanical dimensions:
short card, occupying one slot.

System Requirements:
Software supports Microsoft Windows 2000, 98 and XP.

Ordering Information

E2929B base product
Includes:
- 32/64 bit, 0..133.4 MHz PCI-X protocol checker
- RS-232, USB
- Protocol Checker Graphical User Interface for Windows
- Software media CD

Option #100, PCI-X plug on state analyzer
Includes:
- Plug-on PCI-X State Analyzer piggy pack board
- Analyzer Graphical User Interface for Windows
- 4MB/s fast parallel interface
- Software media CD

Option #200, Performance Optimize[6]
Includes:
- Single user license
- Software media CD

Option #300, PCI-X Exerciser
Includes:
- Customer installable single card license
- Enables on-board 32/64 bit, 0..133 MHz Exerciser hardware
- Exerciser Graphical User Interface for Windows
- Software media CD

When ordering without base product, S/N of the existing E2929A must be notified on purchase order.

Option #310, System Validation[6]
Includes:
- Single user license
- Graphical User Interface for Windows . The PCI-X Exerciser (option #300) must be installed
- Software media CD

Option #320, C-API / PPR Library
- customer installable single card license
- enables PPR hardware and C-API interface for one test card
- the PCI-X exerciser option #300 must be installed
- drivers for Windows

Porting support is available to port C-API to Linux, HP-UX or proprietary operating systems. Contact your local sales offices for detailed information.When ordering without base product, S/N of the existing E2929B must be notified on purchase order.

Accessories

External Power Supply E2991A
The External Power Supply supports applications where the Exerciser and Analyzer card should be transparent to the system, you can connect this external power supply to prevent the card from drawing power from its slot.

FuturePlus Analysis Probe[7]
FS2104. Available from Agilent as resell part FSI 60042

[6] with software revison. 2.0

[7] The analysis probe is not an Agilent product. Agilent works closely with FuturePlus to ensure quality products. but the vendor is responsible for functionality, pre-sales and post sales support and warranty

Overview PCI/PCI-X E2920 Series

	PCI Analyzer -protocol checker - 64K state PCI logic analyzer -4MB fast host interface - timing checker -real-time performance measures -GUI - RS-232 interface	**E2940A** compact PCI 32/64 bit 66MHz	**E2925B** PCI 32 bit 33 MHz	**E2928A** PCI 32/64 bit 66 Mhz	**E2929B** PCI-X 32/64 bit 133 MHz -protocol checker -RS-232/USB interface - GUI
Opt.100					**PCI-X Analyzer** - 2M state PCI logic analyzer -4MB fast host interface -real-time performance measures - GUI
Opt..200	**PCI Performance Optimizer**	4M trace memory recommended please order separately		32/64 bit 66 MHz	**PCI-X Performance Optimizer** -post processed and real-time performance analyzer -performance report - GUI
Opt.300	**PCI Exerciser** - master and target -GUI - CLI -512 KB on-board memory	32/64 bit 33 MHz	32 bit 33 MHz	32/64 bit 66 MHz	PCI-X Exerciser - master - target - GUI - 1MB onboard data memory
Opt. 310	**System validation package**	- peer-to-peer test -system memory test - system load test - protocol load test - protocol check - GUI			
Opt.320	**C-API/PPR**	- C-programming interface library -protocol permutation and randomization library			

PCI-PCI-X Bundle:

With the E2997A Agilent also offers a great price on the purchase of the E2928A PCI Card and the E2929B PCI-X card.

Master Target Test Card

The E2922B PCI-X Master target Test card provides validation engineers in the semiconductor industry a fast and predictable way to set up PCI-X protocl compliance of first silicon.

Accessories Agilent Products	**E2940A**	**E2925B**	**E2928A**	**E2929B**
E2991A External power supply		•	•	•
E2993A External Agilent Logic Analyzer Adapter		•	•	
E2994A External general purpose Logic Analyzer Adapter		•	•	
E2995A 155 x 4M trace memory		•	•	
E2996A 155 x 4M trace memory	•	•		
System test library	•	•	•	•

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Related Agilent Literature

- Agilent E2925B 32bit, 33 MHz, PCI Exerciser & Analyzer, technical specifications, p/n 5968-3501E
- Agilent E2928A 32/64bit, 66 MHz, PCI Exerciser & Analyzer, technical specifications, p/n 5968-3506E
- Agilent E2940A CompactPCI Exerciser & Analyzer, technical specifications, P/n 5968-1915E
- Agilent E2922B PCI-X Master Target Card, technical overview, p/n 5968-9577E
- Agilent System Validation Pack, Agilent System Test Library, technical overview, p/n 5968-3500E
- Agilent E2920 Computer Verification Tools, PCI Series, brochure, p/n 5968-9694E
- Intel discusses basic concepts of PCI performance and efficient use of PCI with the Agilent E2920 series, case study, p/n 5988-0448E
- HP NSD stabilizes server designs quickly and completely with the Agilent E2920 PCI Series, case study, p/n 5968-6948E
- HP HSTC speeds high-end server testing and reduces engineering costs with the Agilent E2920 PCI Series, case study, p/n 5968-6949E
- Agilent E2920 Verification Tools, PCI Series gives Altera Corporation competitive Advantage, case study, p/n 5968-4191E

You can find the current literature and software at:
www.agilent.com/find/pci_products

For more information, please visit us at:
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